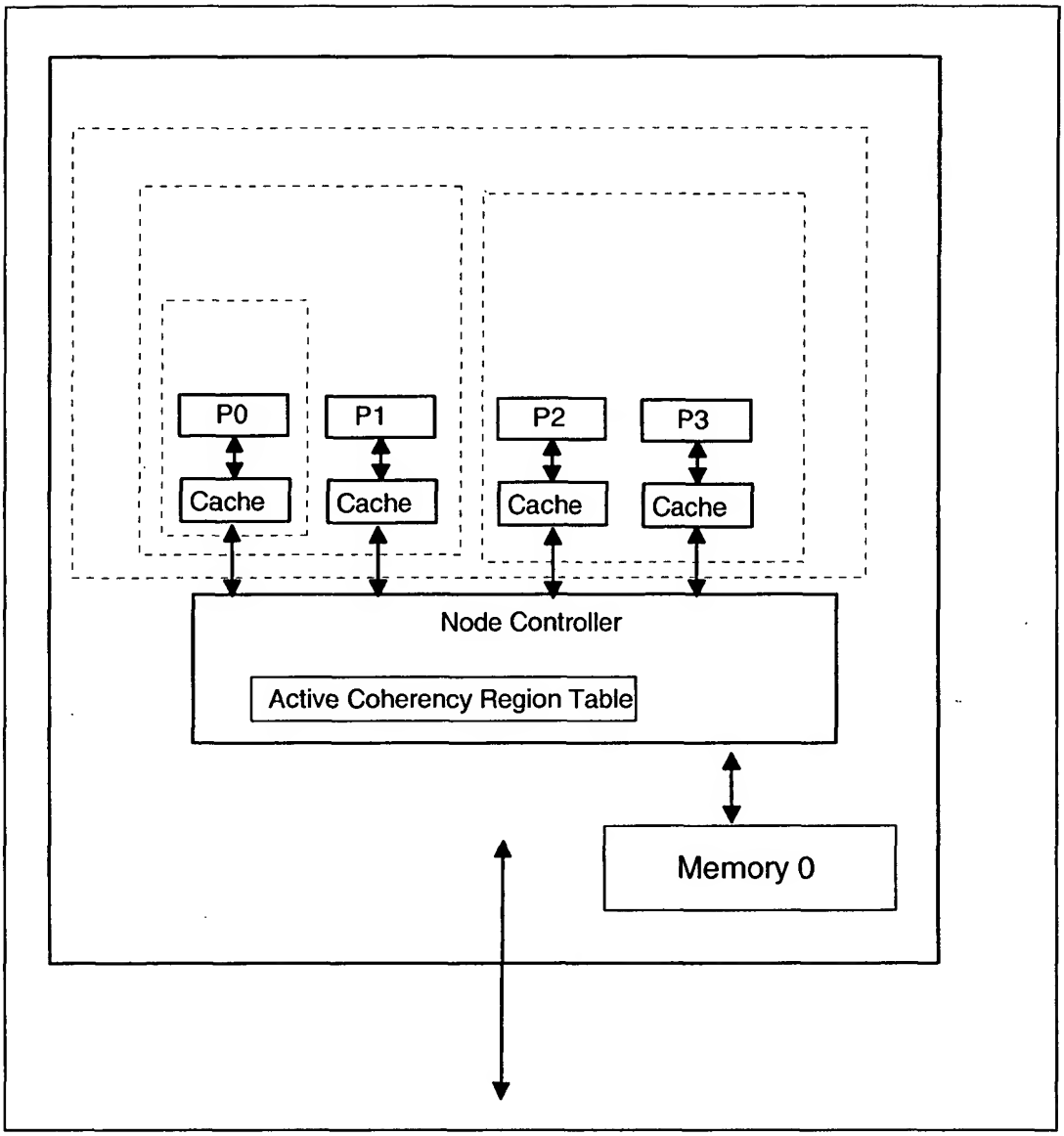
P0
P1
P2
P3
Cache
Cache
Cache
Cache
Node Controller
Active Coherency Region Table
Memory 0

FIGURE 1

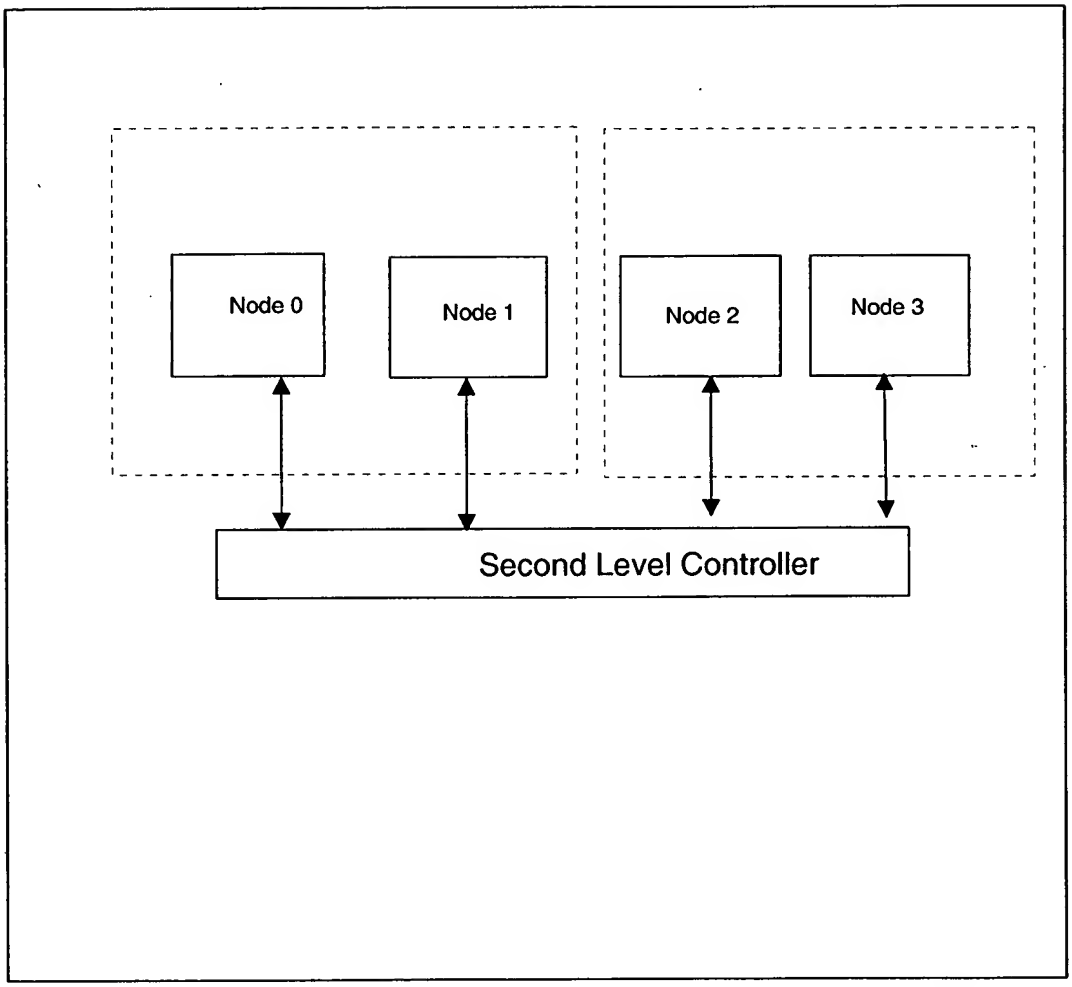

FIGURE 2.

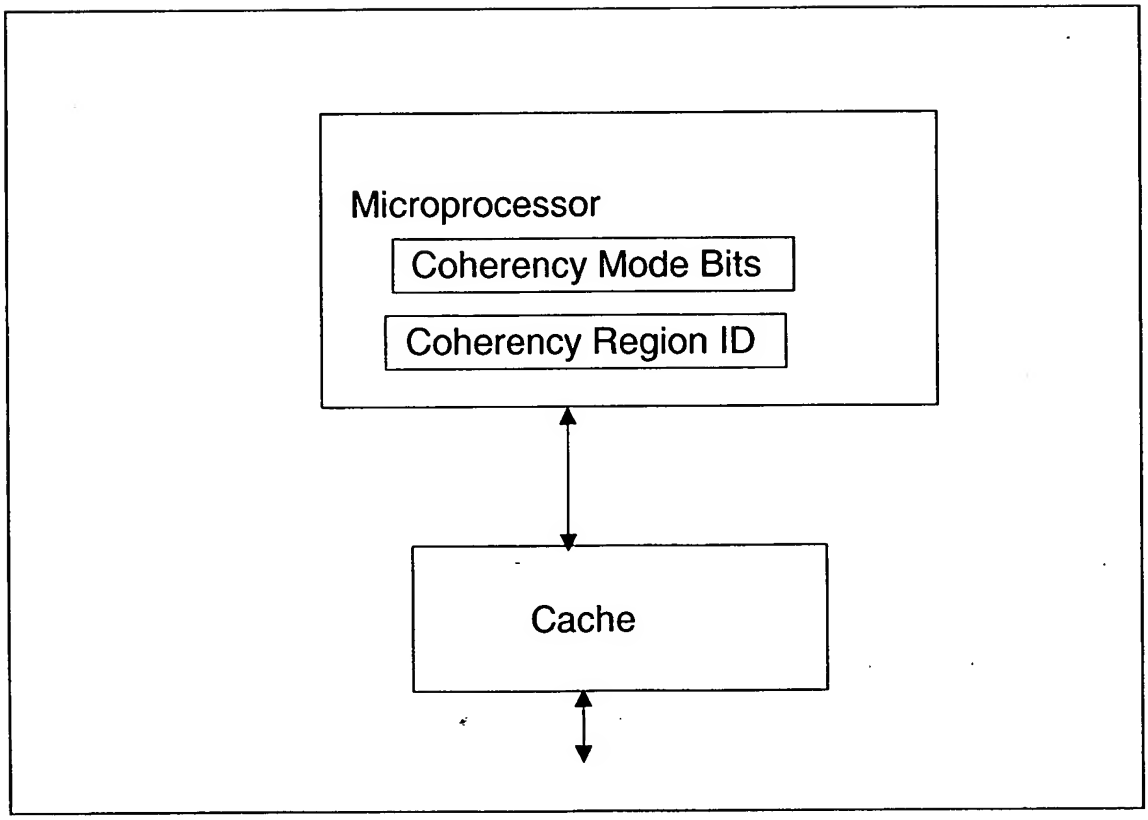
Microprocessor
Coherency Mode Bits
Coherency Region ID
Cache

FIGURE 3.

Originating Processor	Mode Bit Setting	Node Controller Action: Transmit Transaction to the following processors and/or second level controllers:
P0	"000"	Do not forward transaction
P0	"001"	Processor P1
P0	"010"	All Processors in originating node.
P0	"1xx"	All Processors in originating node and second level controllers
P1	"000"	Do not forward transaction
P1	"001"	Processor P0
P1	"010"	All Processors in originating node.
P1	"1xx"	All Processors in originating node and second level controller
P2	"000"	Do not forward transaction
P2	"001"	Processor P3
P2	"010"	All Processors in originating node.
P2	"1xx"	All Processors in originating node and second level controllers
P3	"000"	Do not forward transaction
P3	"001"	Processor P2
P3	"010"	All Processors in originating node.
P3	"1xx"	All Processors in originating node and second level controllers

"1xx" is used to describe a 1 in the first bit position and any combination of bit in the second and third bit positions.

FIGURE 4.

Originating Node	Mode Bit Setting	Second Level Controller Action: Transmit transaction to the following nodes:
0	"0xx"	Not Applicable
0	"101"	Node 1
0	"111"	All Nodes
1	"0xx"	Not Applicable
1	"101"	Node 0
1	"111"	All Nodes
2	"0xx"	Not Applicable
2	"101"	Node 3
2	"111"	All Nodes
3	"0xx"	Not Applicable
3	"101"	Node 2
3	"111"	All Nodes

FIGURE 5.

Partition ID	Coherency Mode	Processors Allowed for Dispatch (Node:Processors)	
0	"000"	(0:P2)	
1	"000"	(1:P1)	
2	"001"	(2:P0)(2:P1)	
3	"010"	(3:P0)(3:P1)(3:P2)(3:P3)	
4	"010"	(0:P0)(0:P1)(0:P2)(0:P3)	
5	"101"	(2:P0)(2:P1)(2:P2)(2:P3) (3:P0)(3:P1)(3:P2)(3:P3)	
6	"111"	Any processor on any of the 4 nodes	

FIGURE 6.

Active Coherency Region Table

Entry #	Coherency Region ID
0	4
1	7
2	23
N	6

FIGURE 7.